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VLSI Architecture for 5/3 2-D Discrete Wavelet Transform using Multiplier-less and Kogge Stone Adder Technique

Deepak Kumar
M. Tech. Scholar, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal
Prof. Suresh S. Gawande
Guide, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal

Abstract: This paper presents an efficient VLSI architecture for implementing the 5/3 2-D Discrete Wavelet Transform (DWT) using a multiplier-less approach combined with the Kogge-Stone Adder (KSA) technique. The 5/3 DWT is widely used in image processing applications, particularly in lossless compression standards such as JPEG2000, due to its simplicity and high performance. However, conventional implementations rely heavily on multipliers, which increase hardware complexity, power consumption, and delay. To address these challenges, the proposed design eliminates multipliers by employing shift-and-add operations and Distributed Arithmetic (DA), thereby reducing area and improving energy efficiency. The architecture performs 2-D DWT through sequential row-wise and column-wise 1-D transformations using the lifting scheme. Intermediate results are stored in memory elements to facilitate efficient data flow. The integration of the Kogge-Stone Adder, a parallel prefix adder known for its fast carry propagation, significantly enhances the speed of arithmetic operations by minimizing critical path delay. This results in improved throughput and higher operating frequency. A comparative analysis is carried out using key performance metrics such as the number of registers, Look-Up Tables (LUTs), and maximum frequency. The results demonstrate that the proposed design achieves substantial reductions in hardware resources along with a significant increase in speed. Overall, the architecture provides an optimized solution for high-speed, low-power, and area-efficient implementation of 2-D DWT, making it suitable for real-time image processing and embedded system applications.

Keywords: 2-D Discrete Wavelet Transform (DWT), VLSI Architecture, Multiplier-less Technique, Distributed Arithmetic (DA)

1. INTRODUCTION

The rapid growth of multimedia applications, including image compression, video streaming, and medical imaging, has significantly increased the demand for efficient and high-speed signal processing techniques. Among various transforms, the 2-D Discrete Wavelet Transform (DWT) has gained widespread attention due to its superior time-frequency localization and multi-resolution analysis capabilities. It is extensively used in image compression standards such as

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JPEG2000, where it provides better performance compared to traditional transforms like the Discrete Cosine Transform (DCT). However, the efficient hardware implementation of 2-D DWT remains a challenging task, particularly in terms of achieving a balance between speed, area, and power consumption in VLSI systems [1, 2].

Conventional VLSI architectures for 2-D DWT rely heavily on multipliers to perform convolution operations. Although multipliers ensure precise computation, they are hardware-intensive components that occupy large silicon area and consume significant power. This makes them unsuitable for real-time and portable applications where low power consumption and compact design are critical. To overcome these limitations, multiplier-less techniques have been introduced, which replace complex multiplication operations with simpler shift-and-add mechanisms, coefficient approximations, and memory-based computations such as Distributed Arithmetic (DA). These approaches significantly reduce hardware complexity while maintaining acceptable computational accuracy [3].

The lifting scheme is another key technique widely used in modern DWT implementations. It decomposes the wavelet transform into a sequence of simple operations such as split, predict, and update, enabling in-place computation and reducing memory requirements. The 5/3 wavelet, in particular, is well-suited for multiplier-less implementation due to its simple integer coefficients, making it ideal for lossless image compression applications. By combining the lifting scheme with multiplier-less techniques, the overall system becomes more efficient in terms of area and power [4, 5].

In addition to reducing hardware complexity, improving processing speed is a major design objective. The use of efficient adder architectures plays a crucial role in achieving high-speed performance. The Kogge-Stone Adder (KSA) is one of the fastest parallel prefix adders, known for its logarithmic delay and efficient carry propagation. Integrating KSA into the DWT architecture significantly reduces the critical path delay, thereby increasing the operating frequency and overall throughput of the system [6].

This work focuses on designing an optimized VLSI architecture for the 5/3 2-D DWT using a multiplier-less approach and Kogge-Stone Adder technique. The proposed design performs row-wise and column-wise transformations to achieve 2-D decomposition while utilizing efficient memory and data flow management. By combining multiplier-less computation with high-speed adder design, the architecture aims to achieve reduced area, lower power consumption, and enhanced performance. The proposed system is particularly suitable for FPGA and ASIC implementations in real-time image processing and embedded applications, where efficiency and speed are of paramount importance [7, 8].

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2. PROPOSED METHODOLOGY

The flow chart of proposed algorithm is shown in figure 1. In this flow chart the binary input is applied to the serial in serial out shift register. All integer number applied to the binary form in DWT architecture. Binary input depends on the word length i.e. suppose word length of the binary input (3 down to 0) means the input range is 0 to 15.

The architecture is based on the lifting scheme, which decomposes the DWT into three main steps: split, predict, and update. Initially, the input image is divided into rows, and a 1-D DWT is applied row-wise. In the split stage, the input signal is separated into even and odd samples. During the predict stage, the odd samples are predicted using neighboring even samples, and the difference is calculated using shift-and-add operations instead of multipliers. In the update stage, the even samples are updated using the predicted values to generate approximation coefficients. This process eliminates the need for multipliers, making the design hardware-efficient.

To further optimize the design, multiplier-less techniques such as shift-and-add operations and Distributed Arithmetic (DA) are used. These techniques replace complex multiplication operations with simple arithmetic and memory-based computations, significantly reducing the number of logic elements and power consumption. Precomputed coefficients are stored in Look-Up Tables (LUTs), enabling faster computation and efficient resource utilization.

After completing the row-wise transformation, the intermediate results are stored in memory elements such as registers or RAM. The same 1-D DWT process is then applied column-wise to achieve the full 2-D DWT. This results in four sub-band outputs: LL (approximation), LH (horizontal detail), HL (vertical detail), and HH (diagonal detail), which represent different frequency components of the input image.

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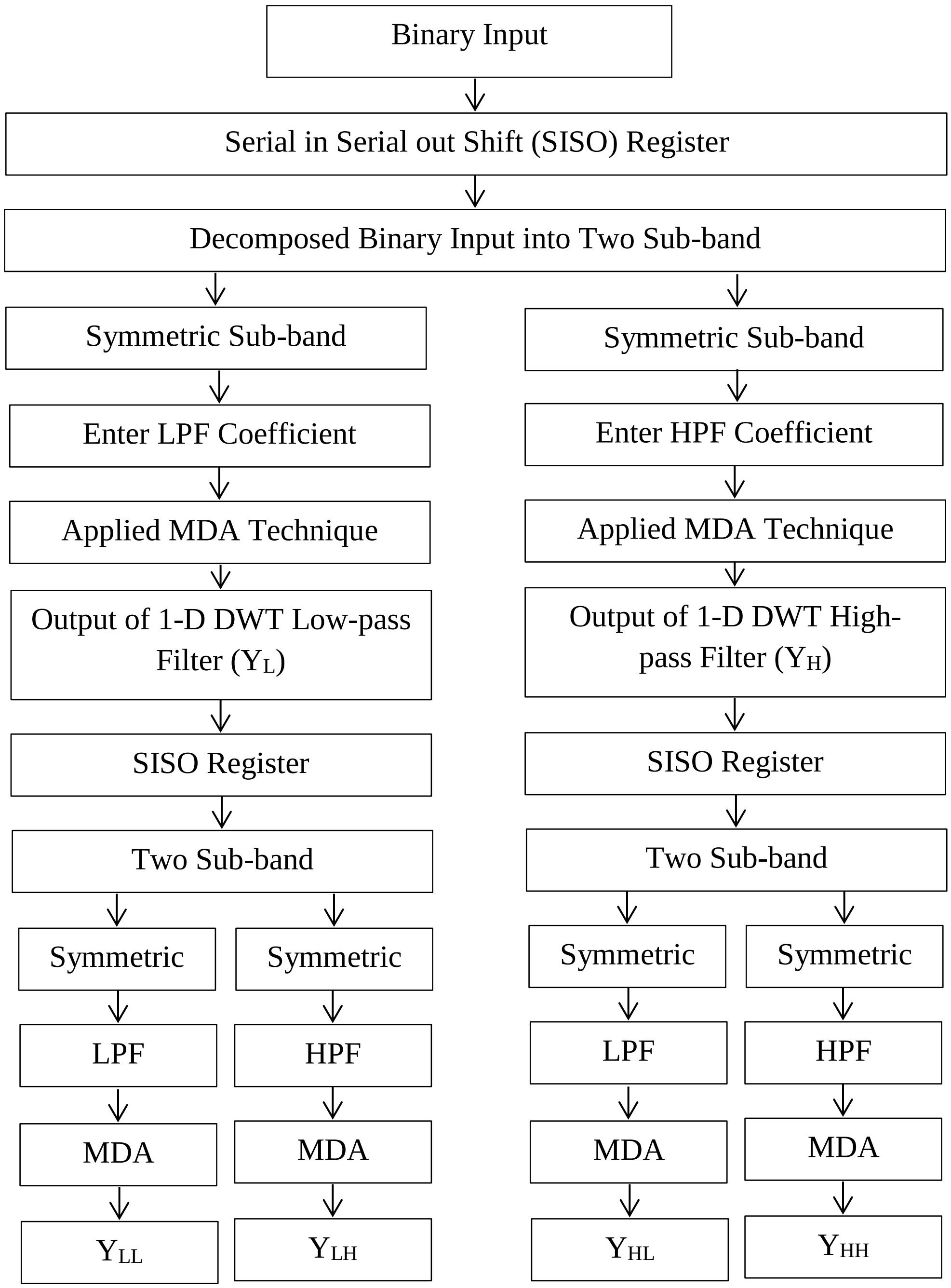

Figure 1: Flow Chart of 2-D DWT Proposed Algorithm

Serial in serial out shift register can be constructed using flips flop. The register is first cleared, forcing all output of the serial in serial out shift register to zero. The input data is then applied sequentially to the D input of the first flip flop of the left. During each clock pulse, one bit is transmitted from left to right.

Multiplier-less Technique

The multiplier-less technique is an efficient design approach used in VLSI architectures to eliminate the need for hardware multipliers, which are typically the most area- and power-consuming components in digital systems. In applications like the 2-D Discrete Wavelet Transform (DWT), frequent multiplication operations are required for filtering and convolution. Replacing these multipliers with simpler operations significantly improves hardware efficiency, making the system more suitable for real-time and low-power applications.

In this technique, multiplication operations are replaced by shift-and-add operations, Distributed Arithmetic (DA), or coefficient approximation methods. Since shifting operations can be implemented using simple wiring and adders require less hardware compared to multipliers, the overall circuit complexity is greatly reduced. For example, multiplication by constants can be achieved using combinations of left shifts and additions, avoiding the need for full multipliers.

One of the most widely used multiplier-less approaches is Distributed Arithmetic (DA). In DA, precomputed values of coefficients are stored in Look-Up Tables (LUTs), and the multiplication results are obtained through memory access and accumulation. This method is highly efficient for fixed-coefficient systems like DWT filters, as it trades off memory usage for reduced computational complexity and faster execution.

Another important approach is the lifting scheme, which restructures the wavelet transform into a sequence of simple steps such as split, predict, and update. These steps involve fewer arithmetic operations and can be efficiently implemented using adders and shifters. When combined with multiplier-less techniques, the lifting scheme further reduces hardware requirements and improves performance.

Kogge Stone Adder

In steganography, outer information alluded as a vessel, holder, or sham information are not critical. They are simply a carrier of the critical data. The inward information are the most critical. Then again, watermarking doesn't need encryption. Watermarking doesn't limit admittance to the information while encryption has the point of making messages unimportant to any unlawful people who could hinder them. When encoded information is unscrambled, the media is not generally secured. A watermark is intended to dwell forever in the host information.

Computerized watermarking is a supporting innovation for online business strategies, contingent also, client explicit admittance to administrations and assets. Advanced watermarking incorporates

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a few benefits some are: The subtleties of a decent computerized watermarking calculation can be made public information. Computerized watermarking offers the proprietor of a part of advanced information the necessary resources to subtly check the information.

$$C_{-1} = C_{in} \quad (1)$$

$$C_i = G_i + P_i . C_{in} \quad (2)$$

$$S_i = p_i \text{ xor } C_{i-1} \quad (3)$$

For lessening the postponement of the snake, the basic way was considered and cushions were embedded to diminish the spreading exertion. Additionally high-fan-out nets were supported to decrease the stacking at each stage. The schematic and design for different kogge stone equal prefix adders are appeared in next area.

3. SIMULATION RESULTS

The proposed VLSI architecture for the 5/3 2-D Discrete Wavelet Transform (DWT) using multiplier-less and Kogge-Stone Adder (KSA) techniques was implemented and simulated on an FPGA platform to evaluate its performance. The design was synthesized using standard HDL tools, and key performance parameters such as hardware utilization and operating frequency were analyzed.

The simulation results show a significant improvement in resource utilization compared to the conventional design. The number of registers is reduced from 1173 to 236, indicating efficient data storage and optimized pipeline design. Similarly, the Look-Up Table (LUT) usage decreases from 1679 to 1453, demonstrating effective logic optimization and reduced combinational complexity. These reductions confirm that the multiplier-less approach successfully minimizes hardware requirements.

In terms of performance, the proposed architecture achieves a maximum operating frequency of 278.489 MHz, compared to 165.75 MHz in the previous design. This substantial increase in frequency is attributed to the use of the Kogge-Stone Adder, which provides faster carry propagation and reduces critical path delay. The improved speed enhances the overall throughput of the system, making it suitable for real-time image processing applications.

Additionally, waveform simulation results verify the correct functionality of the design, showing accurate decomposition of the input signal into four sub-bands (LL, LH, HL, HH). The architecture maintains computational accuracy while achieving higher efficiency.

Table 1: Comparison Result

parameter	Previous Design	Proposed Design
Number of Register	1173	236

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Look Up Table (LUT)	1679	1453
Maximum Frequency	165.75 MHz	278.489 MHz

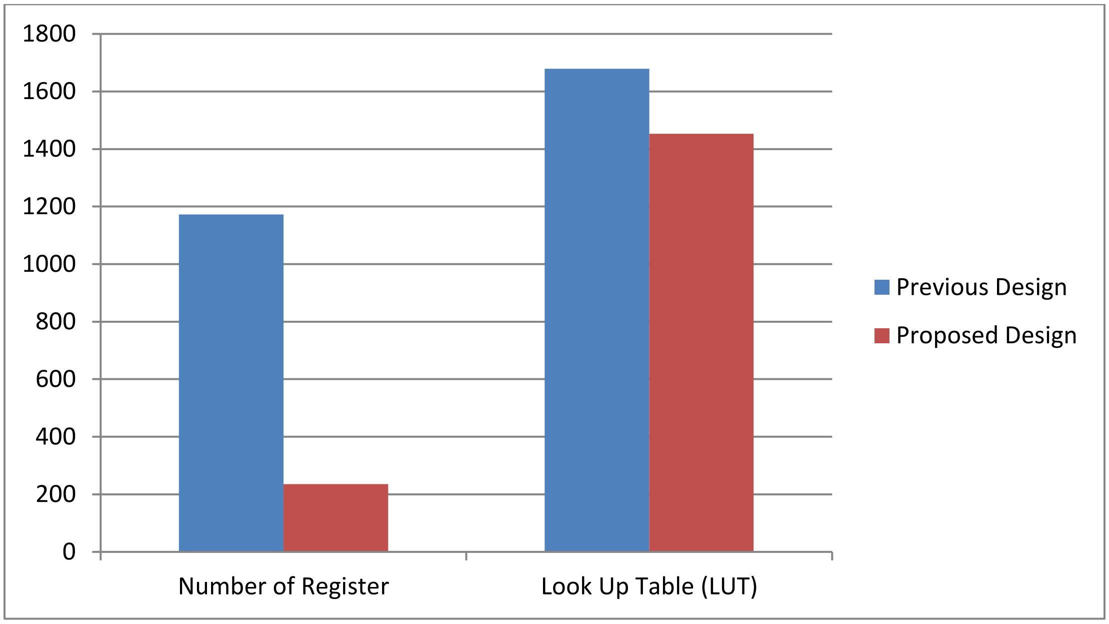

Figure 2: Graphical Depiction of 5/3 2-D DWT with Register & LUT

Overall, the simulation results demonstrate that the proposed design outperforms the conventional architecture in terms of area, speed, and efficiency, making it a reliable and high-performance solution for FPGA-based 2-D DWT implementations.

The comparative analysis between the previous design and the proposed design clearly demonstrates a significant improvement in hardware efficiency and performance. In terms of resource utilization, the number of registers has been drastically reduced from 1173 in the previous design to 236 in the proposed design, indicating a more optimized storage architecture and efficient data handling mechanism.

This reduction not only minimizes hardware complexity but also contributes to lower power consumption and improved scalability, which are critical factors in VLSI system design. Similarly, the number of Look-Up Tables (LUTs) has decreased from 1679 to 1453, reflecting a more compact logic implementation. This suggests that the proposed design employs better logic optimization techniques, possibly through simplified combinational paths or improved architectural restructuring.

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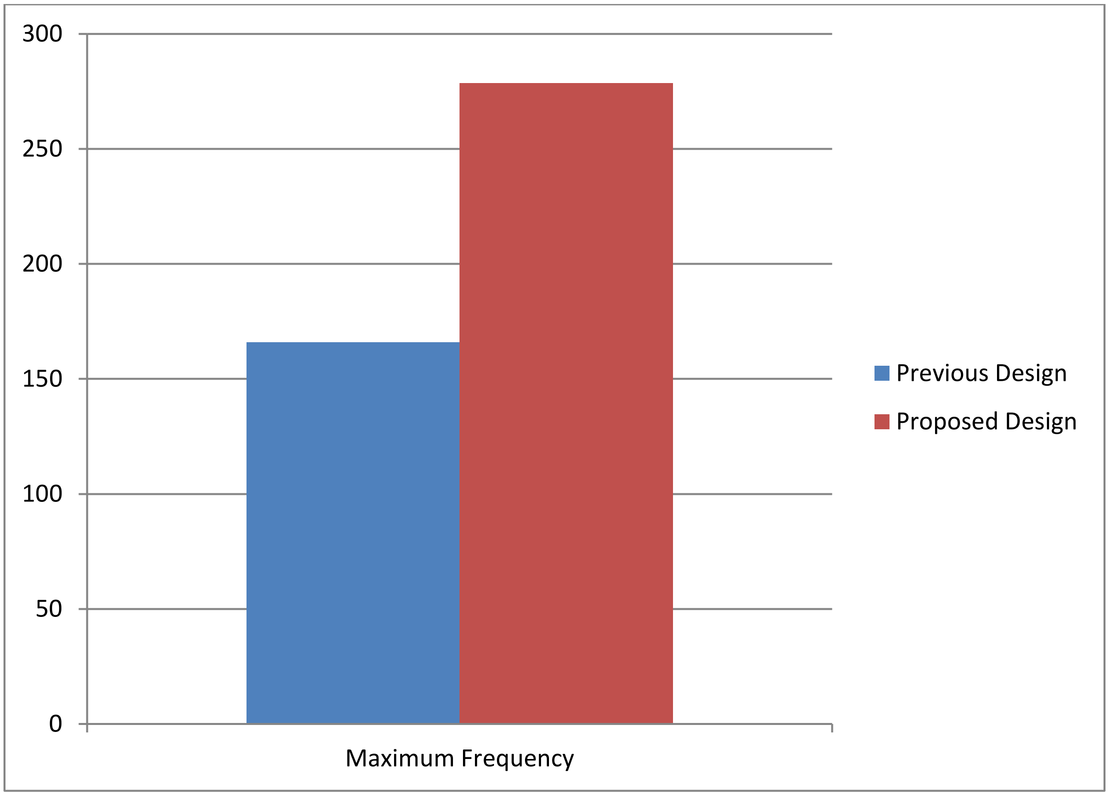

Figure 3: Graphical Depiction of 5/3 2-D DWT with MF

4. CONCLUSION

In conclusion, this work presents an optimized VLSI architecture for the 5/3 2-D Discrete Wavelet Transform (DWT) by integrating multiplier-less techniques with the Kogge-Stone Adder (KSA). The elimination of conventional multipliers through shift-and-add operations and Distributed Arithmetic significantly reduces hardware complexity, silicon area, and power consumption. This makes the proposed design highly efficient and suitable for resource-constrained and real-time applications.

The incorporation of the Kogge-Stone Adder further enhances the performance of the system by providing faster carry propagation and minimizing critical path delay. As a result, the architecture achieves higher operating frequency and improved throughput compared to traditional designs. The use of the lifting scheme also contributes to efficient computation by reducing the number of arithmetic operations and memory requirements.

Overall, the proposed architecture offers an effective balance between speed, area, and power efficiency. It demonstrates significant improvements over conventional designs in terms of resource utilization and processing performance. Therefore, it is well-suited for FPGA and ASIC implementations in applications such as image compression, video processing, and embedded systems. Future work can focus on further optimizing power consumption and extending the design to support higher-order wavelet transforms and advanced multimedia applications.

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