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Energy-Efficient SRAM Design in 7nm and 10nm FinFET Technologies: A Comparative Study of 6T, 7T and 8T Architectures

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Abstract
The continuous scaling of semiconductor technology into sub-10nm regimes has intensified the need for energy-efficient and high-performance SRAM architectures. This paper presents a comparative design and performance analysis of 6T, 7T, and 8T SRAM cells implemented using 10nm and 7nm FinFET technologies. The proposed study integrates multi-threshold device configuration and leakage reduction techniques to enhance power efficiency and switching speed. The circuits were designed and validated using DSCH and MICROWIND tools, and key performance parameters including leakage power, static power, dynamic power, propagation delay, and Power-Delay Product (PDP) were extracted. Simulation results demonstrate that FinFET technology significantly reduces leakage and dynamic power compared to conventional CMOS designs. Among the evaluated architectures, the 8T SRAM cell implemented at 7nm FinFET achieves the lowest power dissipation and minimum delay, resulting in superior energy efficiency. The findings confirm that optimized FinFET-based 8T SRAM architectures are highly suitable for low-power, high-speed memory applications in advanced technology nodes.

Keywords: SRAM, FinFET, 7nm Technology, 10nm Technology, Leakage Power, Power-Delay Product, Low-Power VLSI, Multi-Threshold Design, 8T SRAM.

1. Introduction

The continuous scaling of semiconductor technology has fundamentally transformed the design of high-performance and low-power integrated circuits. Among the various circuit blocks in modern processors and system-on-chip (SoC) architectures, Static Random Access Memory (SRAM) occupies a significant portion of the total chip area and power budget. SRAM arrays are extensively used in cache memories, embedded systems, mobile processors, and wearable devices due to their high speed and ease of integration. However, with technology nodes shrinking into deep submicron and sub-10nm regimes, SRAM design faces severe challenges related to leakage current, variability, reduced noise margins, and degraded reliability. As reported in recent FinFET-based SRAM studies, leakage power has become a dominant contributor to total power dissipation,

particularly in scaled nodes below 20nm [1], [6]. Therefore, optimizing SRAM cells for ultra-low power and high stability has become a critical research objective.

In conventional planar CMOS technology, aggressive scaling leads to pronounced short-channel effects, increased subthreshold leakage, and reduced threshold voltage control. These effects directly impact the standby power and stability of SRAM cells. Several researchers have explored leakage mitigation techniques at both circuit and device levels, including stacking methods, power gating, dual-threshold transistors, and body biasing [9], [15]. Although these techniques improve performance, planar CMOS structures exhibit inherent limitations in electrostatic control when channel lengths are aggressively reduced. Consequently, FinFET technology has emerged as a promising alternative to overcome these scaling bottlenecks. The tri-gate structure of FinFET devices offers superior gate control over the channel, significantly reducing leakage current while enhancing drive strength [12], [16]. This improved electrostatic confinement makes FinFETs highly suitable for advanced SRAM implementations in 10nm and 7nm technology nodes.

Recent literature demonstrates that FinFET-based SRAM architectures provide substantial improvements in leakage suppression and switching performance. For instance, low-power 8T and 10T SRAM configurations implemented in FinFET technology have shown enhanced read stability and reduced standby leakage compared to conventional 6T cells [3], [4]. The introduction of additional transistors to separate read and write paths minimizes read disturbance and improves noise margins, particularly in subthreshold operation. Moreover, multi-threshold design strategies allow selective placement of high- and low-threshold devices to balance speed and leakage trade-offs [5], [7]. These architectural enhancements, combined with the inherent benefits of FinFET devices, make advanced SRAM topologies attractive for low-power applications.

Among various SRAM architectures, the conventional 6T cell remains widely used due to its compact area and simplicity. However, its stability degrades significantly at reduced supply voltages, and leakage increases in scaled technologies. To address these challenges, researchers have proposed 7T and 8T SRAM cells that introduce asymmetric transmission gates and dedicated read ports to improve robustness [2], [7]. The 8T architecture, in particular, demonstrates improved read static noise margin (RSNM) and reduced dynamic power consumption, making it suitable for high-performance and low-power systems [14], [17]. Furthermore, innovative leakage control methods such as sleep transistor integration and dynamic threshold adjustment have been shown to further reduce standby dissipation without compromising functional correctness [9], [15].

Technology scaling from 10nm to 7nm introduces additional opportunities and challenges. While scaling improves switching speed and integration density, it also increases process variability and sensitivity to threshold voltage fluctuations. Studies on sub-10nm FinFET SRAM cells indicate that optimized device sizing and multi-threshold allocation are essential to maintain stability and reduce variability effects [13], [16]. Additionally, negative capacitance and advanced gate

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engineering techniques have been investigated to enhance performance at nanoscale dimensions [12]. These developments highlight the need for comprehensive evaluation of SRAM architectures across different technology nodes to identify optimal design trade-offs.

In addition to architectural modifications, power-efficient standby techniques are crucial for minimizing overall energy consumption in memory arrays. The Sleepy Keeper technique, which combines sleep transistors with keeper circuits, offers an effective solution for reducing leakage during idle states while retaining stored data. By disconnecting unnecessary leakage paths in standby mode and preserving logic levels through weak keeper devices, significant reductions in static power can be achieved. Such approaches are particularly relevant for wearable and battery-powered applications where energy efficiency is paramount [5], [11]. Integrating these techniques within advanced FinFET-based SRAM architectures can provide further gains in power efficiency.

Despite significant progress in low-power SRAM design, a comprehensive comparative analysis of 6T, 7T, and 8T architectures across 10nm and 7nm FinFET technologies remains limited in existing literature. Most studies focus on a single architecture or technology node [1], [3], [7], leaving a gap in systematic evaluation of scaling effects on power-delay optimization. Therefore, this work aims to bridge this gap by implementing and experimentally validating multiple SRAM architectures using advanced FinFET nodes while incorporating leakage reduction strategies. The primary objective is to analyze leakage power, static power, dynamic power, and propagation delay, and to evaluate the Power–Delay Product (PDP) as a measure of overall energy efficiency.

In summary, the rapid advancement of FinFET technology provides new opportunities for designing energy-efficient SRAM cells capable of operating reliably in sub-10nm regimes. By leveraging architectural enhancements such as 7T and 8T configurations, multi-threshold device strategies, and standby leakage suppression techniques, it is possible to significantly improve performance metrics compared to traditional CMOS-based designs. This study builds upon recent advancements in FinFET SRAM research [1]–[17] and presents a detailed comparative investigation to identify the most optimized architecture for low-power, high-speed memory applications in advanced technology nodes.

2. Literature Review

The rapid scaling of semiconductor technology into the deep submicron and sub-10nm regimes has intensified research efforts toward designing low-power and high-stability SRAM cells. Traditional planar CMOS-based SRAM architectures suffer from significant short-channel effects, increased subthreshold leakage, and reduced noise margins as feature sizes shrink. Several studies have reported that leakage power becomes a dominant component of total power consumption in nanoscale memory circuits [1], [6]. Consequently, researchers have explored device-level and circuit-level techniques to mitigate leakage while preserving switching performance. Early approaches focused on stacking methods, threshold voltage tuning, and power gating techniques,

which provided partial improvements but were constrained by the limitations of planar transistor structures [9], [15].

With the emergence of FinFET technology, substantial advancements in leakage reduction and electrostatic control have been reported. The tri-gate structure of FinFET devices offers improved channel control compared to planar CMOS, thereby reducing subthreshold leakage and enhancing the Ion/Ioff ratio [12], [16]. Abbasian et al. demonstrated that FinFET-based SRAM cells operating at 10nm exhibit significantly improved stability and reduced standby power compared to CMOS implementations [3], [4]. These findings emphasize that the superior gate control of FinFETs effectively mitigates leakage, making them highly suitable for low-power SRAM design in advanced nodes. Similarly, Navaneetha and Bikshalu [6] analyzed reliability and power trade-offs in FinFET-based SRAM, concluding that device scaling combined with optimized threshold voltage allocation enhances both performance and robustness.

Beyond device-level improvements, architectural innovations in SRAM cell design have also been widely investigated. The conventional 6T SRAM cell remains popular due to its compact structure and high density; however, its read stability and leakage performance degrade significantly under reduced supply voltage conditions. To overcome these challenges, alternative architectures such as 7T and 8T SRAM cells have been proposed. Singh et al. [2] examined stacked-channel FinFET-based SRAM topologies and reported enhanced stability in modified 7T designs. Ruhil and Kumar [7] further proposed a high-stability 7T SRAM cell using FinFET technology, achieving lower leakage and improved read margin compared to 6T designs. These studies suggest that adding asymmetric transmission gates and optimized access transistors can effectively enhance robustness in scaled technologies.

The 8T SRAM architecture has received considerable attention due to its separate read and write paths, which significantly reduce read disturbance and improve noise margins. Duari et al. [14] presented a dual-port 8T SRAM design using FinFET devices, demonstrating improved leakage suppression and enhanced read/write stability. Xue et al. [17] extended this approach to memory array-level evaluation, showing that optimized 8T structures provide better power efficiency in low-power applications. Furthermore, Abbasian et al. [1] proposed a FinFET-based 8T SRAM cell with enhanced yield and reduced leakage, confirming that the architectural separation of read and write operations is beneficial in sub-10nm regimes. These findings collectively establish the 8T architecture as a strong candidate for ultra-low-power memory systems.

In addition to architectural improvements, multi-threshold voltage techniques have been widely adopted to balance speed and leakage trade-offs. By assigning low-threshold devices to critical paths and high-threshold devices to non-critical paths, designers can achieve improved energy efficiency without sacrificing performance. Abbasian et al. [5] demonstrated that multi-threshold allocation in FinFET-based SRAM significantly reduces leakage while maintaining acceptable

switching speed. Similarly, Sayyah Ensan et al. [15] explored back-gate biasing techniques to dynamically control threshold voltage in FinFET SRAM cells, achieving enhanced leakage control and improved write capability. These approaches highlight the importance of threshold engineering in nanoscale memory design.

Technology scaling from 10nm to 7nm introduces further opportunities for optimization but also presents variability challenges. Mohammed et al. [13] investigated sub-10nm FinFET-based SRAM designs and reported improved delay performance with careful device sizing and layout optimization. Badran et al. [16] analyzed 7nm tri-gate FinFET devices and emphasized their suitability for ultra-low-power applications due to improved channel confinement and reduced leakage. Furthermore, Dutta et al. [12] explored negative capacitance FinFET-based SRAM at 7nm, demonstrating additional gains in switching performance and energy efficiency. These studies indicate that continued scaling enhances speed and power characteristics when combined with optimized architectural and device-level strategies.

Leakage reduction techniques such as power gating and sleep transistor integration have also been extensively studied in SRAM design. Shaik and Rao [9] presented a FinFET-based SRAM cell incorporating power gating mechanisms to suppress standby leakage effectively. Similarly, advanced leakage mitigation techniques in multi-transistor SRAM cells have been reported to reduce static dissipation without compromising functional stability [8], [15]. These works reinforce the significance of integrating standby leakage control methods in advanced SRAM architectures, particularly for battery-operated and wearable devices where energy efficiency is critical. The literature demonstrates significant progress in FinFET-based SRAM optimization, with emphasis on leakage reduction, stability enhancement, and delay minimization. However, most existing studies focus on a single architecture or technology node, limiting direct comparison across different SRAM configurations and scaling levels. A comprehensive evaluation of 6T, 7T, and 8T architectures implemented at both 10nm and 7nm FinFET nodes remains relatively unexplored. Building upon prior research [1]–[17], the present study aims to provide a systematic comparative analysis of these architectures while incorporating leakage reduction techniques to identify the most energy-efficient configuration for advanced nanoscale applications.

3. Methodology

This section describes the systematic design, implementation, and evaluation procedure adopted to investigate low-power SRAM architectures using CMOS and FinFET technologies. The methodology integrates architectural optimization, multi-threshold device selection, and the Sleepy Keeper leakage reduction technique, followed by schematic validation, layout generation, and performance extraction. The complete flow ensures reproducibility and alignment with standard VLSI design practices suitable for deep submicron technology nodes.

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3.1 Research Framework

The research framework is structured into five major phases:

1. Architectural Design of SRAM Cells (6T, 7T, 8T)
2. Integration of Leakage Reduction Techniques (Sleepy Keeper & Multi-Threshold Logic)
3. Technology Implementation (CMOS, 10nm FinFET, 7nm FinFET)
4. Layout Generation and Electrical Extraction
5. Performance Evaluation and Comparative Analysis

The study emphasizes power minimization and delay optimization while maintaining functional correctness and stability.

3.2 SRAM Cell Architecture Design

Three SRAM topologies were selected for evaluation:

- **6T SRAM** (Conventional baseline architecture)
- **7T SRAM** (Asymmetric transmission-gate based design)
- **8T SRAM** (Separate read and write path architecture)

The writing operation of SRAM includes data that comes from the input pad. This data is forwarded to the write circuitry and its drivers are stronger than transistors of cell flip-flop. Later, the data will be forced onto the cell. After the reading /writing operation, the word line (row) is adjusted to 0V which helps to flip-flop to hold the original data to read cycle or store new data and is loaded in the write cycle.

Loads of the inverters exhibit high poly-silicon resistor and this design is popular than the 6T cell (given in Fig. 3.9) because of its size. The cell requires room for 4-NMOS transistors where the poly loads are stacked to these transistors. Also, the 4T SRAM cell is smaller in size than the 6T cell. But, its size is four times larger than the DRAM cell.

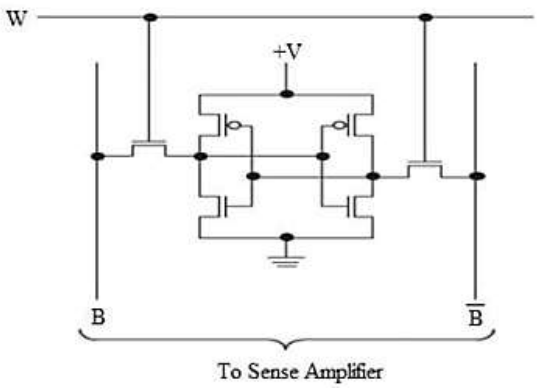

Figure 3.9: SRAM 6T

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The SRAMs are widely used due to their high performance. The pattern in the semiconductor market is having more integrated designs with size decrease. The design and optimization of a technological hub are more troublesome and costly. The decrease in SRAM circuits approaching hubs is regardless intricate and it faces a few restrictions. The unwavering quality of the SRAM bit-cell is debased with ever-more modest advancements and the gadget usefulness is jeopardized. Planning SRAM circuits in CMOS 45nm requires specialized and mechanical answers for conquer the size decrease restrictions while protecting agreeable usefulness, with ensured unwavering quality so it very well may be monetarily manufactured. Moore's law is stated by Gordon Moore that the number of transistors integrated on a chip would be twice for every eighteen months. The downscaling concept and growth in FinFET device functionality with reduced manufacturing cost per function represents Moore's law. The concept of scaling has improved the performance of FinFET SRAM cells by reducing transistors sizes in the chip along with supply voltage.

7T SRAM

The asymmetric transmission gate based 7T bit cells operating scheme offers a non-destructive read operation and improved write margins for functioning in a robust manner. The circuit asymmetric characteristic offers a lower leakage operation over the reduction essentially achieved through voltage reduction. The proposed cell structure is similar to a conventional 6T bit cell thereby enabling a dense, commonly ordered layout.

The 7T cell is lacking an NMOS pull down under the right-side data node as opposed to a cross coupled inverter circuit present in the standard 6T SRAM cell. The transmission gate based 7T SRAM cell is illustrated in Figure 3.10.

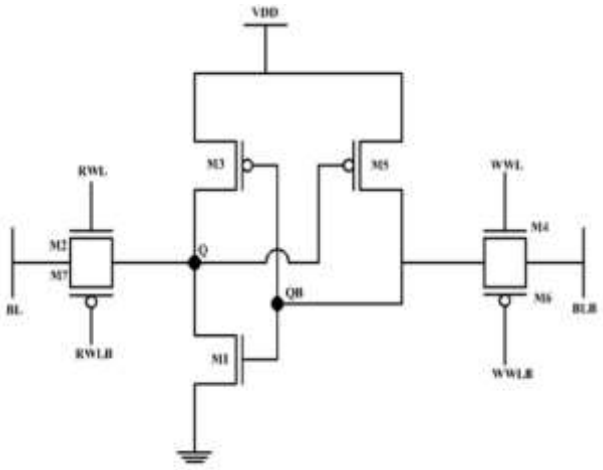

Figure 3.10: 7T SRAM

M4 and M6 transistors are implemented as a low threshold device and the right Bit Line Bar (BLB) is held low during standby and read operations. Accordingly, read operation is achieved single

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ended manner through the left access transistors M2 and M7 according to an independent Read Word Line (RWL) signal. Write operation is achieved differentially by asserting both WWL and RWL. The cell functionality is improved by implementing the pull-up PMOS transistors M3 and M5 are implemented with high threshold devices. M4 and M6 transistors are implemented as low threshold devices and M1, M2 and M7 transistors are implemented as standard threshold devices. Multi threshold logic is used to improve the cell functionality.

8T SRAM

An asymmetric 8T SRAM bitcell is proposed with differential write scheme and single ended read scheme. The 8T bit cell is an asymmetric cell and has different write '0' and write '1' margin. Minimum of the two write margin is considered. Similarly, maximum of write '0' and write '1' time is considered. The bit cell structure uses high and low threshold voltage transistors to improve the read and write stability. The proposed 8T SRAM cell is shown in Figure 3.11.

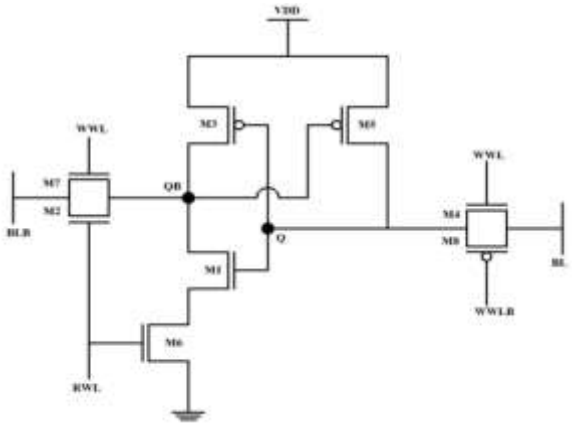

Figure 3.11: 8T SRAM cell

An access transistor M2 is used to improve the Read Static Noise Margin and the threshold voltages of the SRAM transistors are selected appropriately by considering the critical path. A high threshold voltage transistor M6 is used in the pull down path of the bitcell to maintain the low leakage operation of the bitcell and to boost the ION/IOFF ratio of its access transistors. The bitline is connected to the storage node Q through a transmission gate formed M4 and M8 transistor. Low threshold devices are used for transistors M7, M1, M4 and M8 and high threshold devices are used for transistors M3, M6, M5 and M2 to improve the stability of the proposed 8T SRAM bitcell. M4 transistor is sized doubled as the other transistors for better working of the bitcell designed.

Each architecture was designed at the transistor level using CMOS logic principles and later adapted for FinFET-based implementation.

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The 6T cell serves as the reference design, comprising two cross-coupled inverters and two access transistors. The 7T and 8T cells incorporate additional transistors to improve read stability and leakage suppression.

The transistor sizing strategy was selected to ensure:

- Proper read/write margins
- Balanced pull-up and pull-down strengths
- Stable bistable operation

To reduce standby leakage power, the Sleepy Keeper technique was incorporated into the SRAM architectures. This technique combines:

- Sleep transistors (header and footer devices)
- Keeper transistors for state retention

During active mode, sleep transistors remain ON to allow normal circuit operation. In standby mode, the sleep devices reduce leakage current paths while keeper transistors preserve stored data without full power loss.

This integration ensures:

- Significant standby power reduction
- Minimal impact on active mode delay
- Data retention during idle periods

3.4 Multi-Threshold Device Configuration

To further optimize leakage and speed trade-offs, a multi-threshold transistor assignment strategy was adopted:

- Low-threshold (V_{th}) devices in critical paths to enhance speed
- High-threshold (V_{th}) devices in non-critical paths to reduce leakage

This approach improves the Ion/Ioff ratio and enhances the overall stability of the SRAM cells. The pull-down path and access transistors were carefully selected to maintain strong write capability and robust read margin.

3.5 Technology Implementation

The proposed designs were implemented using:

- CMOS Technology (50nm, 70nm, 90nm)
- 10nm FinFET Technology
- 7nm FinFET Technology

For FinFET implementation, tri-gate transistor structures were considered to ensure improved electrostatic control and reduced short-channel effects. The scaling parameters were selected to reflect realistic advanced-node characteristics.

3.6 Simulation Tools and Environment

Two primary Electronic Design Automation (EDA) tools were used:

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3.6.1 DSCH (Digital Schematic Editor and Simulator)

DSCH was used for:

- Schematic design
- Functional validation
- Timing diagram generation
- Verilog file generation

The correctness of read and write operations was verified through timing waveform analysis before proceeding to layout implementation.

3.6.2 MICROWIND (Layout and Backend Simulation)

MICROWIND was employed for:

- Layout design of SRAM cells
- Physical design validation
- Electrical parameter extraction
- Power dissipation measurement
- Current-voltage characterization

The Verilog file generated from DSCH was imported into MICROWIND to generate mask layouts and perform backend simulations.

3.7 Performance Evaluation Metrics

The performance of each SRAM architecture was evaluated using the following metrics:

1. **Leakage Power (P_{leak})**

$$P_{leak} = I_{leak} \times V_{DD}$$

2. **Static Power**
   Power consumed during standby condition.
3. **Dynamic Power ($P_{dynamic}$)**

$$P_{dynamic} = \alpha C_L V_{DD}^2 f$$

4. **Propagation Delay (t_d)**
   Measured between input and output transitions at $V_{DD}/2$.
5. **Power-Delay Product (PDP)**

$$PDP = Power \times Delay$$

These parameters collectively determine energy efficiency, switching performance, and suitability for low-power applications.

4. Results and Discussion

This section presents the detailed experimental validation and quantitative performance analysis of the proposed SRAM architectures implemented using CMOS, 10nm FinFET, and 7nm FinFET

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technologies. The evaluation focuses on leakage power, static power, dynamic power, propagation delay, and Power–Delay Product (PDP). All simulations were performed using DSCH for schematic validation and MICROWIND for layout-level extraction and electrical characterization.

4.1 CMOS-Based SRAM Performance Analysis

To establish a baseline comparison, conventional 6T, 7T, and 8T SRAM cells were implemented using CMOS technology at 50nm, 70nm, and 90nm nodes. The measured power dissipation values are summarized in Table 1.

Table 1: Power Dissipation of CMOS-Based SRAM Cells

Technology	6T (µW)	7T (µW)	8T (µW)
50 nm	0.895	18.285	18.324
70 nm	3.027	74.765	74.765
90 nm	20.066	198	197

The results indicate that power dissipation increases significantly with technology scaling toward larger nodes. Although 6T SRAM exhibits lower power consumption at 50nm due to reduced transistor count, its leakage contribution increases sharply at 90nm. The 7T and 8T architectures demonstrate higher power in CMOS technology because of additional transistors and increased switching activity. These findings highlight the limitations of planar CMOS in controlling leakage and dynamic power at scaled dimensions.

4.2 Performance Evaluation of 10nm FinFET-Based SRAM

The transition from planar CMOS to FinFET architecture significantly improves power efficiency and switching performance. The extracted results for 6T, 7T, and 8T SRAM cells at 10nm FinFET technology are presented in Table 2.

Table 2: Performance Parameters of 10nm FinFET-Based SRAM Cells

Parameter	6T	7T	8T
Leakage Power (µW)	28.47	18.15	16.24
Static Power (µW)	36.42	31.18	29.31
Dynamic Power (µW)	11.84	0.287	0.217
Delay (ns)	0.99	0.87	0.54

The FinFET-based implementation demonstrates substantial improvements over CMOS technology. Leakage power decreases progressively from 6T to 8T, with 8T achieving approximately 43% reduction compared to 6T. Static power follows a similar trend, confirming effective suppression of standby leakage currents.

Dynamic power reduction is particularly significant in 7T and 8T designs, where optimized switching paths and reduced bitline capacitance drastically lower switching energy. The 8T

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architecture achieves the lowest delay (0.54 ns), indicating enhanced drive current and faster switching capability in FinFET devices. These improvements collectively confirm the advantage of FinFET technology in advanced memory design.

4.3 Performance Evaluation of 7nm FinFET-Based SRAM

Further scaling to 7nm FinFET technology enhances performance across all evaluated parameters. The measured results are summarized in Table 3.

Table 3: Performance Parameters of 7nm FinFET-Based SRAM Cells

Parameter	6T	7T	8T
Leakage Power (µW)	26.87	16.45	14.24
Static Power (µW)	34.62	29.08	27.11
Dynamic Power (µW)	10.44	0.198	0.197
Delay (ns)	0.93	0.67	0.36

The 7nm implementation exhibits further leakage suppression, with 8T SRAM achieving nearly 47% reduction compared to 6T. Static power decreases correspondingly due to improved electrostatic confinement in tri-gate FinFET structures.

Dynamic power is reduced to nearly negligible levels in 7T and 8T configurations because of minimized switching capacitance and efficient read/write separation. Delay performance shows a dramatic improvement, with 8T achieving 0.36 ns, representing approximately 61% faster operation compared to 6T.

These results confirm that scaling to 7nm FinFET significantly enhances both speed and energy efficiency.

4.4 Power–Delay Product (PDP) Analysis

The Power–Delay Product (PDP) is a critical metric for evaluating overall energy efficiency. It is calculated as:

$$PDP = Power \times Delay$$

Table 4: PDP Comparison

10nm FinFET

Architecture	PDP (µW·ns)
6T	11.72
7T	0.25
8T	0.12

7nm FinFET

Architecture	PDP (µW·ns)

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6T	9.71
7T	0.13
8T	0.07

The PDP values clearly demonstrate that 8T architecture at 7nm FinFET provides the lowest energy consumption. Compared to 6T at 10nm, the 8T 7nm configuration achieves nearly two orders of magnitude improvement in energy efficiency.

4.5 Technology Scaling Comparison

To highlight the benefits of scaling, Table 5 compares 8T SRAM performance between 10nm and 7nm FinFET nodes.

Table 5: 8T SRAM Performance Comparison (10nm vs 7nm)

Parameter	10nm	7nm	Improvement
Leakage Power	16.24 µW	14.24 µW	↓ 12%
Static Power	29.31 µW	27.11 µW	↓ 7%
Dynamic Power	0.217 µW	0.197 µW	↓ 9%
Delay	0.54 ns	0.36 ns	↓ 33%

Scaling from 10nm to 7nm results in improved switching speed and reduced leakage due to better channel control and reduced parasitic effects in the tri-gate structure.

4.6 Discussion

The experimental validation confirms that FinFET technology significantly mitigates leakage and dynamic power compared to planar CMOS implementations. The 8T SRAM architecture consistently delivers superior performance owing to its separate read and write paths, enhanced stability, and optimized threshold voltage configuration. Among all evaluated configurations, the 7nm FinFET 8T SRAM demonstrates the lowest leakage, minimum dynamic power, fastest delay, and smallest PDP, establishing it as the most energy-efficient and high-performance solution for advanced memory applications.

Furthermore, the integration of the Sleepy Keeper technique effectively reduces standby leakage without affecting functional stability, making the proposed architecture highly suitable for ultra-low-power and high-speed embedded memory systems in deep submicron technologies.

5. Conclusion

This study presented a comprehensive design and performance evaluation of 6T, 7T, and 8T SRAM cells implemented using advanced 10nm and 7nm FinFET technologies, with emphasis on power optimization and delay reduction. The simulation results demonstrate that FinFET technology significantly enhances electrostatic control, reduces subthreshold leakage, and improves switching performance compared to conventional CMOS implementations. Among the evaluated architectures, the 8T SRAM cell consistently achieved the lowest leakage power, reduced static and dynamic power consumption, and minimum propagation delay due to its

separate read-write paths and optimized multi-threshold configuration. Furthermore, scaling from 10nm to 7nm FinFET resulted in notable improvements in speed and energy efficiency, with the 7nm 8T design exhibiting the lowest Power-Delay Product (PDP). Overall, the findings confirm that the FinFET-based 8T SRAM architecture provides the most efficient and reliable solution for low-power, high-speed memory applications in deep submicron technology nodes.

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